2022-EE-103

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**Lab Report # 2**

Task no 1

Part a:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| A | B | C | ~C |  | (A+B) | ~(AB) |  | (A+B)+(~(AB)) |  | (A+B)+(~C) | (A+B).((A+B)+(~AB)) |
| 0 | 0 | 0 | 1 |  | 0 | 1 |  | 1 |  | 1 | 0 |
| 0 | 0 | 1 | 0 |  | 0 | 1 |  | 1 |  | 0 | 0 |
| 0 | 1 | 0 | 1 |  | 1 | 1 |  | 0 |  | 0 | 0 |
| 0 | 1 | 1 | 0 |  | 1 | 1 |  | 0 |  | 1 | 0 |
| 1 | 0 | 0 | 1 |  | 1 | 1 |  | 0 |  | 0 | 0 |
| 1 | 0 | 1 | 0 |  | 1 | 1 |  | 0 |  | 1 | 0 |
| 1 | 1 | 0 | 1 |  | 1 | 0 |  | 1 |  | 0 | 1 |
| 1 | 1 | 1 | 0 |  | 1 | 0 |  | 1 |  | 1 | 1 |

Part B: module full\_adder(

input logic a,

input logic b,

input logic c,

output logic sum,

output logic carry,

);

sum = (a ^ b) ^ c;

assign carry = (a & b) | (c & (a ^ b));

endmodule

listing no 5;

module full\_adder\_tb();

logic a1, b1, c1, sum1, carry1;

full\_adder uut (

.a(a1),

.b(b1),

.c(c1),

.sum(sum1),

.carry(carry1)

);

initial begin

// Provide different combinations of the inputs to check the validity of the code

a1 = 0; b1 = 0; c1 = 0;

#10;

a1 = 0; b1 = 0; c1 = 1;

#10;

a1 = 0; b1 = 1; c1 = 0;

#10;

a1 = 0; b1 = 1; c1 = 1;

#10;

a1 = 1; b1 = 0; c1 = 0;

#10;

a1 = 1; b1 = 0; c1 = 1;

#10;

a1 = 1; b1 = 1; c1 = 0;

#10;

a1 = 1; b1 = 1; c1 = 1;

#10;

$stop;

end

endmodule

Task 3 has files

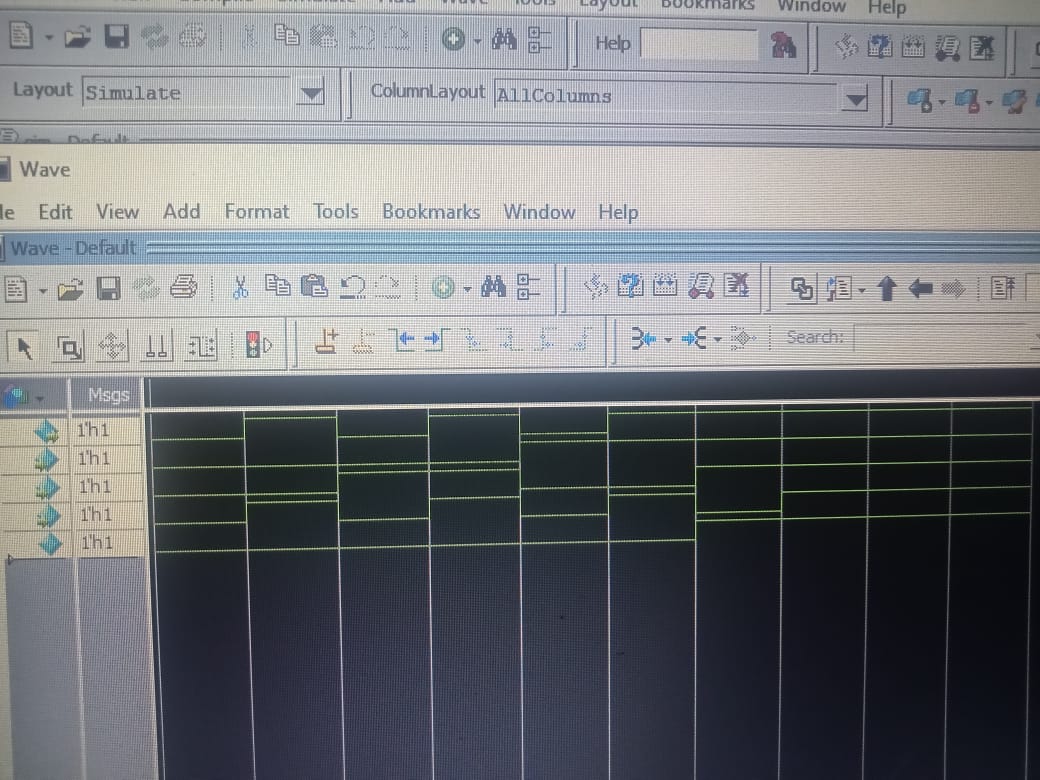




Task no 4

Simulations on questasim are as followed:

Task 1



Task 2 simulation :

